**Date:**

**Ahsanullah University of Science and Technology**

Department of Computer Science and Engineering

Third Year, First Semester Clearance/ Improvement/ Carry Over Examination, Spring 2016

Course No: **CSE 3109** Course Title: **Digital System Design**

Time: 3 Hours Full Marks: 70

**[ There are 7(Seven) questions. Answer any 5(Five) questions.]**

**[*Marks allotted are indicated in the right margin within ‘[ ]’.*]**

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| --- | --- | --- |
| 1.a) | What is the difference between hard-wired control and microprogram control? What are the advantage and disadvantage in each method? | [4] |
| b) | Design an arithmetic circuit that multiplies two fixed-point binary numbers in sign-magnitude representation. The product obtained from the multiplication of two binary numbers whose magnitudes consist of *k* bits each can be up to *2k* bits long. The sign of each number occupies one additional bit. Your design must include the following steps:   1. Equipment Configuration 2. Derivation of Algorithm 3. Flowchart 4. Control state diagram and Sequence of microoperations 5. Data-Processor Specification 6. Design of Hard-wired Control | [10] |
| 2. | The register configuration and flow chart of a digital system that multiplies two unsigned binary numbers by repeated addition method is shown in **Figure 1**.  **Figure 1 :** Multiplication by successive addition.  **B**  **A**  Initial state  x = 1  qm =1  Multiplicand Multiplier  P 0 00  Control  Logic  qm  **P**  A  = 0 x  Product  ≠ 0  P P+B  A A – 1 |  |
| a) | Let A = 0100 and B = 0011. Going through the steps in the flowchart, show that the system returns to the initial state, with register P having the product 1100. | [4] |
| b) | Draw a state diagram for the control and list the register transfers to be executed in each control state. | [5] |
| c) | Draw the block diagram of the data-processor part. | [5] |
| 3.a) | What are the values of status bits C and Z after the subtraction of two unsigned numbers (A – B)? | [2] |
| b) | Deign an arithmetic logic unit with two selection variables S1 and S0, that generates the following arithmetic and logic operations.   |  |  |  |  |  | | --- | --- | --- | --- | --- | | S1 | S0 | Cin = 0 | Cin = 1 | Cin = × (don’t care) | | 0 | 0 | F = A | F = A + 1 | F = A+B (OR) | | 0 | 1 | F = A – B – 1 | F = A – B | F = A⊕B (XOR) | | 1 | 0 | F = B – A – 1 | F = B – A | F = AB (AND) | | 1 | 1 | F = A + B | F = A + B +1 | F = A B (NAND) | | [6] |
| c) | The following register-transfer operations specify a four-state control of the sequence register and decoder type. G is a 2-bit sequence register and T0, T1, T2 and T3 are the outputs of the decoder.  xT0: G G+1  yT0: G 10  zT0: G 11  T1+T2+T3: G G+1  Draw the state diagram of the control and design the sequence register with JK flip-flops. | [6] |
| 4.a) | What is Shift Register? | [2] |
| b) | What are the differences between RAM and ROM? | [3] |
| c) | What is Modified Booth’s algorithm? Explain with example. | [4] |
| d) | Design a 4-bit BCD ripple counter. | [5] |
| 5.a) | What is programmable logic array? Draw the block diagram of PLA. | [3] |
| b) | Show all the steps of Booths algorithm for the following 4 bit numbers:  X = 1001 Y = 0110 | [4] |
| c) | Implement a macrooperation to count the number of 1’s presently stored in processor register *R1* and sets processor register *R2* to that number. For example, if *R1* = 00110101, the microprogram routine counts the four 1’s stored in the register and sets register *R2* to the binary number 100. Your implementation must contain the following steps:   1. Flowchart 2. Symbolic microprogram to count the number of 1’s in *R1* 3. Binary microprogram to count the number of 1’s in *R1* | [7] |
| 6.a) | What is mnemonics? Explain with example. | [2] |
| b) | How much time delay does this SAP -2 subroutine produce?  MVI B,0AH  LOOP1: MVI C,47H  LOOP2: DCR C  JNZ LOOP2  DCR B  JNZ LOOP1  RET | [3] |
| c) | Write a program for SAP-2 that multiplies decimal 12 and 8. | [4] |
| d) | Describe the architecture of SAP-1. | [5] |
| 7.a) | Draw the block diagram and logic diagram of a RAM. | [2] |
| b) | Write the status of the control word **CON** for each of the following states in SAP-1:   1. Address state 2. Increment state 3. Memory state | [3] |
| c) | The inputs to each full-adder circuit of an arithmetic logic unit are according to the following Boolean functions:  Xi = AiBi + (s2s1’s0’)’Ai + s2s1s0’Bi  Yi = s0Bi + s1Bi’(s2s1s0’)’  Zi = s2’Ci  Determine the 12 functions of the ALU. | [4] |
| d) | Draw the LDA and ADD routines of SAP-1 and also draw their fetch and execution timing diagram. | [5] |